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FDMA1032CZ


20V Complementary PowerTrench[®] MOSFET

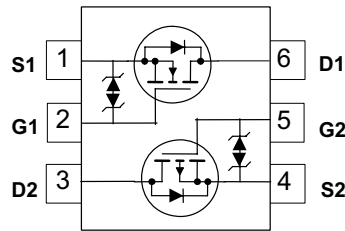
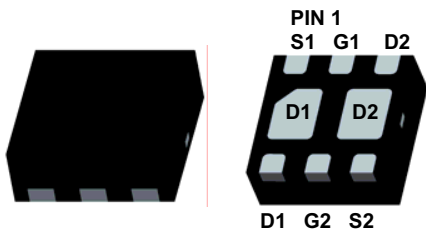


General Description

This device is designed specifically as a single package solution for a DC/DC 'Switching' MOSFET in cellular handset and other ultra-portable applications. It features an independent N-Channel & P-Channel MOSFET with low on-state resistance for minimum conduction losses. The gate charge of each MOSFET is also minimized to allow high frequency switching directly from the controlling device. The MicroFET 2x2 package offers exceptional thermal performance for its physical size and is well suited to switching applications.

Features

- Q1: N-Channel
3.7 A, 20V. $R_{DS(ON)} = 68\text{ m}\Omega @ V_{GS} = 4.5\text{V}$
 $R_{DS(ON)} = 86\text{ m}\Omega @ V_{GS} = 2.5\text{V}$
- Q2: P-Channel
-3.1 A, -20V. $R_{DS(ON)} = 95\text{ m}\Omega @ V_{GS} = -4.5\text{V}$
 $R_{DS(ON)} = 141\text{ m}\Omega @ V_{GS} = -2.5\text{V}$
- Low profile – 0.8 mm maximum – in the new package MicroFET 2x2 mm
- HBM ESD protection level > 2 kV (Note 3) 
- RoHS Compliant
- Free from halogenated compounds and antimony oxides



MicroFET 2x2

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
V _{DS}	Drain-Source Voltage	20	-20	V
V _{GS}	Gate-Source Voltage	±12	±12	V
I _D	Drain Current – Continuous (Note 1a)	3.7	-3.1	A
	– Pulsed	6	-6	
P _D	Power Dissipation for Single Operation (Note 1a) (Note 1b)	1.4		W
		0.7		
T _J , T _{STG}	Operating and Storage Junction Temperature Range	-55 to +150		°C

Thermal Characteristics

R _{θJA}	Thermal Resistance, Junction-to-Ambient	(Note 1a)	86 (Single Operation)	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient	(Note 1b)	173 (Single Operation)	
R _{θJA}	Thermal Resistance, Junction-to-Ambient	(Note 1c)	69 (Dual Operation)	
R _{θJA}	Thermal Resistance, Junction-to-Ambient	(Note 1d)	151 (Dual Operation)	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
032	FDMA1032CZ	7"	8mm	3000 units

Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$ $V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	Q1 Q2	20 -20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C $I_D = -250\ \mu\text{A}$, Referenced to 25°C	Q1 Q2		15 -12		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$	Q1 Q2			1 -1	μA
I_{GSS}	Gate-Body Leakage	$V_{GS} = \pm 12\text{ V}, V_{DS} = 0\text{ V}$	All			± 10	μA
On Characteristics (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$ $V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	Q1 Q2	0.6 -0.6	1.0 -1.0	1.5 -1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C $I_D = -250\ \mu\text{A}$, Referenced to 25°C	Q1 Q2		-4 4		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 4.5\text{ V}, I_D = 3.7\text{ A}$ $V_{GS} = 2.5\text{ V}, I_D = 3.3\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 3.7\text{ A}, T_J = 125^\circ\text{C}$	Q1		37 50 53	68 86 90	m Ω
		$V_{GS} = -4.5\text{ V}, I_D = -3.1\text{ A}$ $V_{GS} = -2.5\text{ V}, I_D = -2.5\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -3.1\text{ A}, T_J = 125^\circ\text{C}$	Q2		60 88 87	95 141 140	
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 3.7\text{ A}$ $V_{DS} = -10\text{ V}, I_D = -3.1\text{ A}$	Q1 Q2		16 -11		S
Dynamic Characteristics							
C_{iss}	Input Capacitance	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	Q1 Q2		340 540		pF
C_{oss}	Output Capacitance		Q1 Q2		80 120		
C_{rss}	Reverse Transfer Capacitance	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	Q1 Q2		60 100		pF
Switching Characteristics (Note 2)							
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 10\text{ V}, I_D = 1\text{ A}, V_{GS} = 4.5\text{ V}, R_{GEN} = 6\ \Omega$	Q1 Q2		8 13	16 24	ns
t_r	Turn-On Rise Time		Q1 Q2		8 11	16 20	
$t_{d(off)}$	Turn-Off Delay Time	$V_{DD} = -10\text{ V}, I_D = -1\text{ A}, V_{GS} = -4.5\text{ V}, R_{GEN} = 6\ \Omega$	Q1 Q2		14 37	26 59	ns
t_f	Turn-Off Fall Time		Q1 Q2		3 36	6 58	
Q_g	Total Gate Charge	$V_{DS} = 10\text{ V}, I_D = 3.7\text{ A}, V_{GS} = 4.5\text{ V}$	Q1 Q2		4 7	6 10	nC
Q_{gs}	Gate-Source Charge		Q1 Q2		0.7 1.1		
Q_{gd}	Gate-Drain Charge	$V_{DS} = -10\text{ V}, I_D = -3.1\text{ A}, V_{GS} = -4.5\text{ V}$	Q1 Q2		1.1 2.4		nC

Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Drain–Source Diode Characteristics and Maximum Ratings							
I_S	Maximum Continuous Source-Drain Diode Forward Current		Q1 Q2			1.1 -1.1	A
V_{SD}	Source-Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 1.1\text{ A}$ (Note 2) $V_{GS} = 0\text{ V}, I_S = -1.1\text{ A}$ (Note 2)	Q1 Q2		0.7 -0.8	1.2 -1.2	V
t_{rr}	Diode Reverse Recovery Time	Q1 $I_F = 3.7\text{ A}, dI_F/dt = 100\text{ A}/\mu\text{s}$	Q1 Q2		11 25		ns
Q_{rr}	Diode Reverse Recovery Charge	Q2 $I_F = -3.1\text{ A}, dI_F/dt = 100\text{ A}/\mu\text{s}$	Q1 Q2		2 9		nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.

(a) $R_{\theta JA} = 86^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper, 1.5 " x 1.5 " x 0.062 " thick PCB. For single operation.

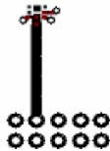
(b) $R_{\theta JA} = 173^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper. For single operation.

(c) $R_{\theta JA} = 69^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper, 1.5 " x 1.5 " x 0.062 " thick PCB. For dual operation.

(d) $R_{\theta JA} = 151^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper. For dual operation.



a) $86^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper.



b) $173^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper.



c) $69^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper.



d) $151^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper.

2. Pulse Test : Pulse Width < 300 us, Duty Cycle < 2.0%

3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics Q1 (N-Channel)

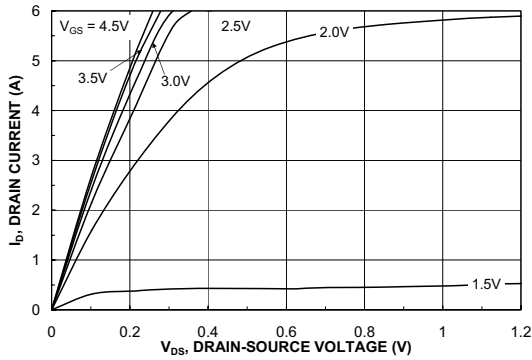


Figure 1. On-Region Characteristics.

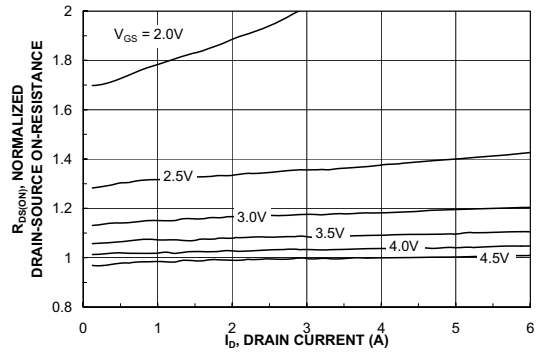


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

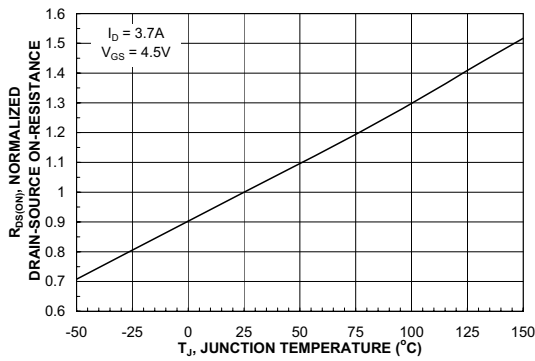


Figure 3. On-Resistance Variation with Temperature.

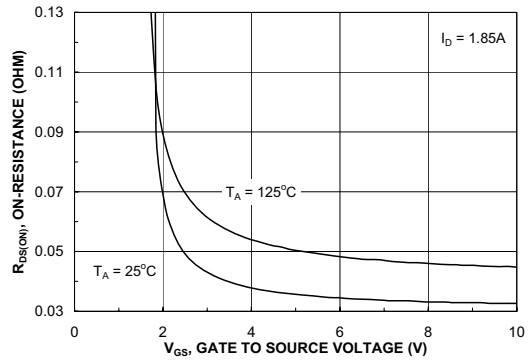


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

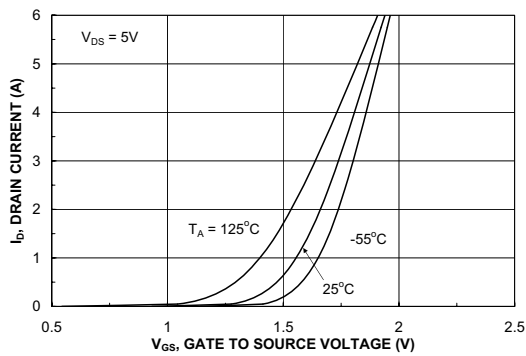


Figure 5. Transfer Characteristics.

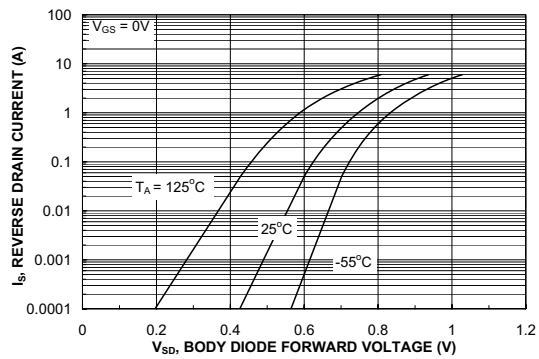


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics Q1 (N-Channel)

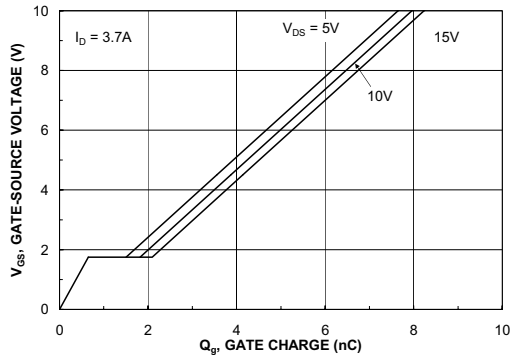


Figure 7. Gate Charge Characteristics.

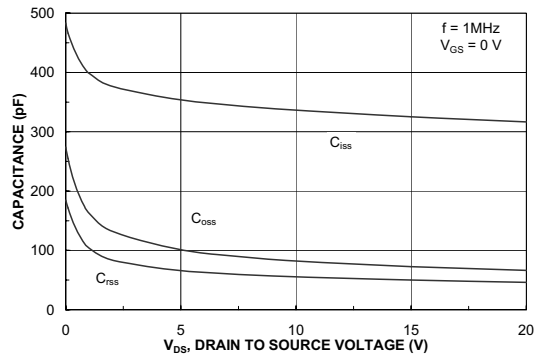


Figure 8. Capacitance Characteristics.

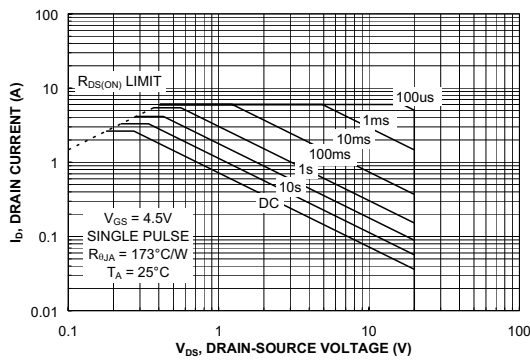


Figure 9. Maximum Safe Operating Area.

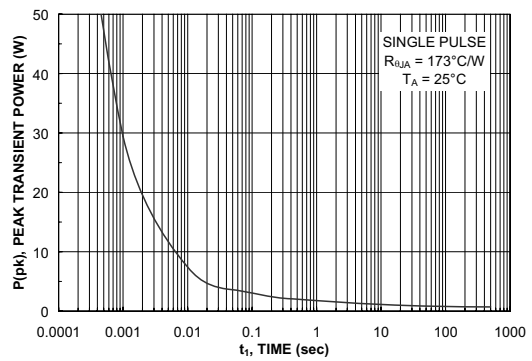


Figure 10. Single Pulse Maximum Power Dissipation.

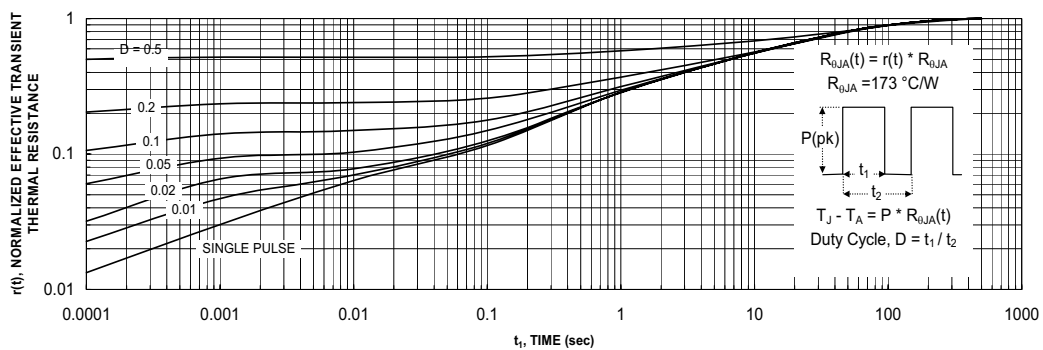


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

Typical Characteristics: Q2 (P-Channel)

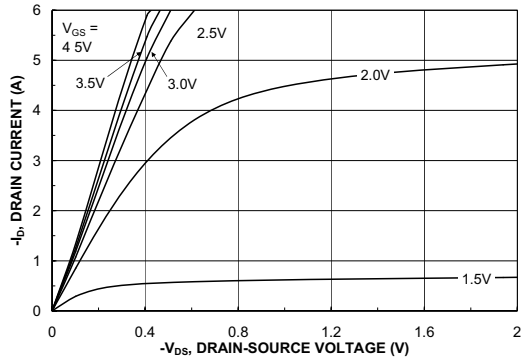


Figure 12. On-Region Characteristics.

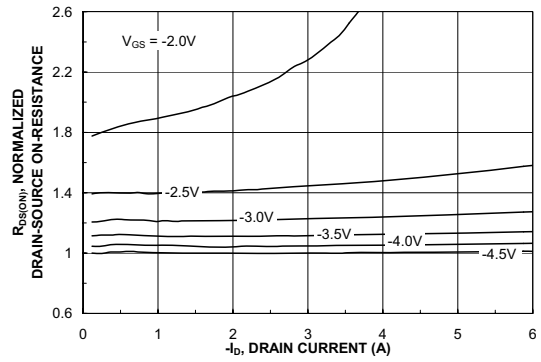


Figure 13. On-Resistance Variation with Drain Current and Gate Voltage.

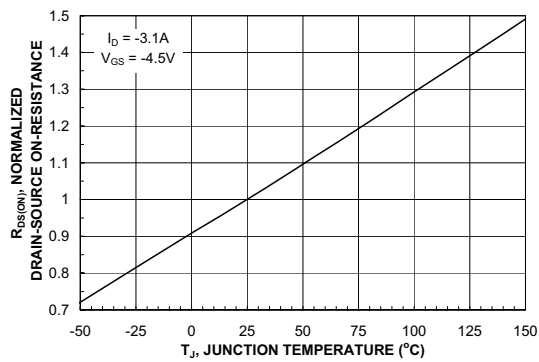


Figure 14. On-Resistance Variation with Temperature.

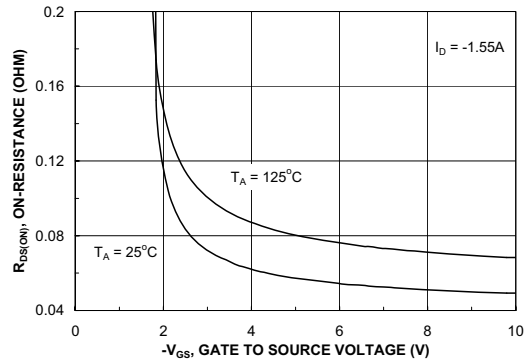


Figure 15. On-Resistance Variation with Gate-to-Source Voltage.

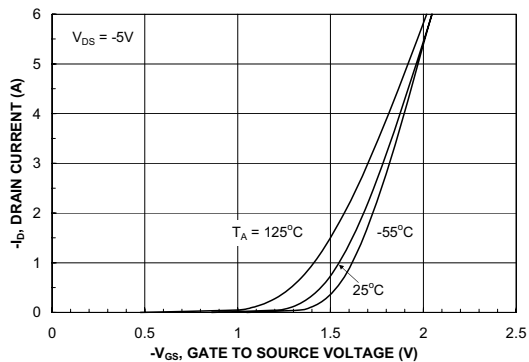


Figure 16. Transfer Characteristics.

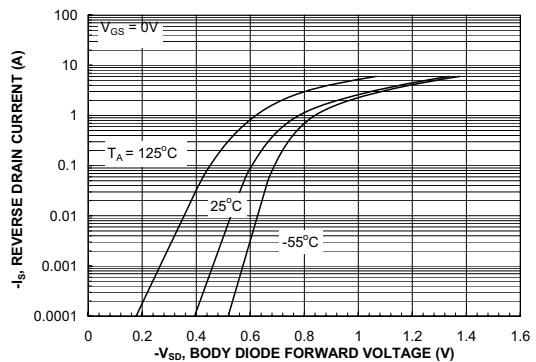


Figure 17. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: Q2 (P-Channel)

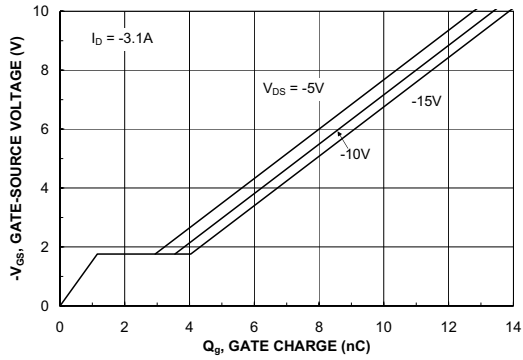


Figure 18. Gate Charge Characteristics.

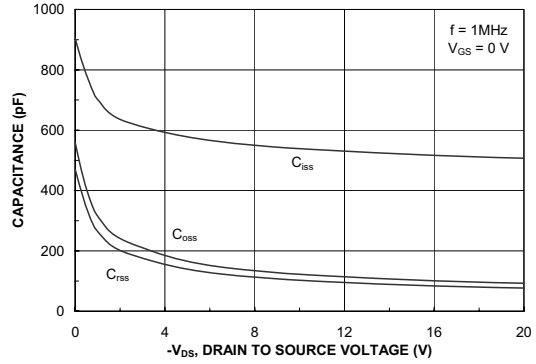


Figure 19. Capacitance Characteristics.

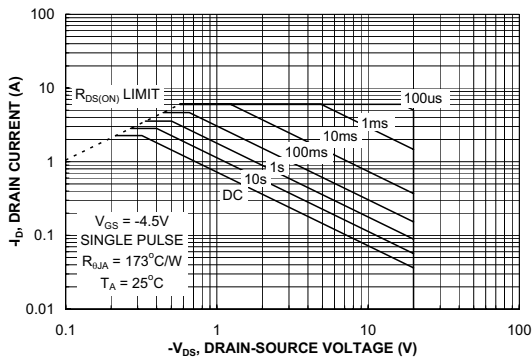


Figure 20. Maximum Safe Operating Area.

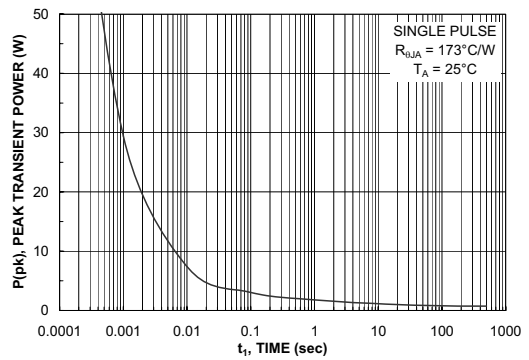


Figure 21. Single Pulse Maximum Power Dissipation.

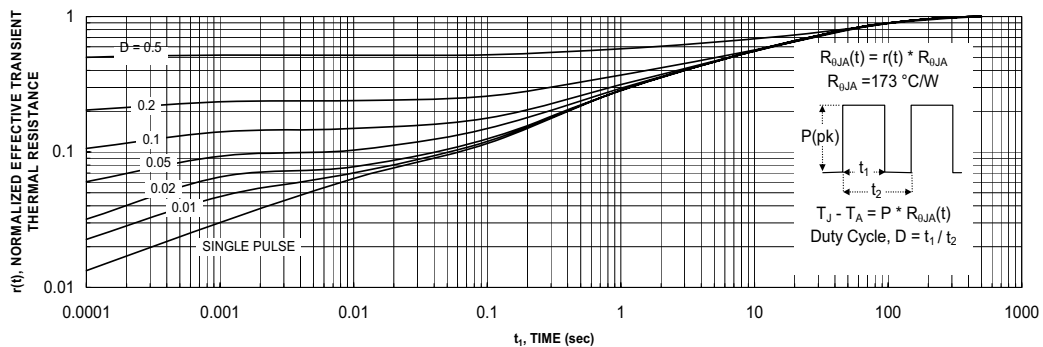
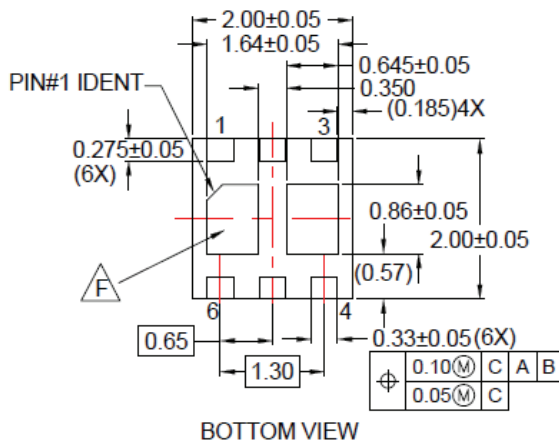
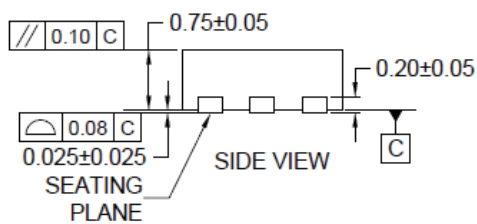
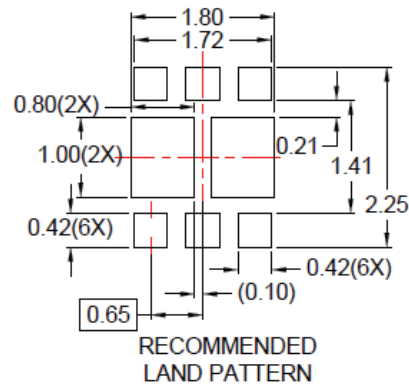
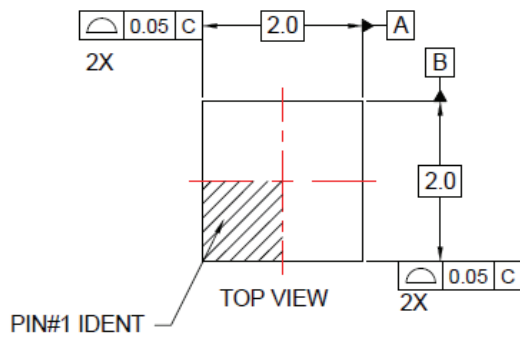


Figure 22. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

Dimensional Outline and Pad Layout



NOTES:

- A. CONFORM TO JADEC REGISTRATIONS MO-229, VARIATION VCCC, EXCEPT WHERE NOTED.
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
 - D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
 - E. DRAWING FILENAME: MKT-UMLP16Erev4
- F. NON-JEDEC DUAL DAP



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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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